In-plane thermal conductivity determination through thermoreflectance analysis and measurements

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A scanning thermoreflectance (TR) technique through which the surface temperature profile of heated thin films may be ascertained and modeled to yield the *in-plane* thermal conductivity (κ_{ip}) is discussed. The TR intensity is shown to be a sensitive function of the film thickness, its thermo-optic materials properties, and the substrate geometry. A reduction in the thermal conductivity of silicon thin films is then demonstrated deploying the technique. A comparison of the estimated conductivity values to those obtained using other methodologies supports the validity of our method and suggests that complete isolation of the thin film from the substrate may not be required for extracting κ_{ip}. © *2011 American Institute of Physics*. [doi:10.1063/1.3647318]

I. INTRODUCTION

A. Anisotropy in thermal conductivity

While substantial progress has been made in the past few years in understanding heat conduction in lower dimensional structures[1,2] such as thin films and nanotubes/nanowires, many issues are still unresolved. There is still difficulty in accurate measurement,[3] and precise understanding of phonon interactions with interfaces/boundaries has not yet been obtained. Additionally, while thermal conductivity (κ) is defined from the ratio of the heat flux to the temperature gradient as a second rank tensor, κ is typically regarded as a scalar and isotropic materials property. Anisotropy in the thermal conductivity is not generally considered even in confined nanostructures such as nanowires.[4] In the case of thin films, a few attempts have been made to correlate possible anisotropies to film and measurement geometry,[5] where, for example, a conductivity variation dependent on the direction heat flow whether cross-plane (κ_{cp}) or in-plane (κ_{ip}), was noted. The discussion has then largely been framed on the basis of the classical[6] interpretation of the κ, as the product of the specific heat capacity (C), the phonon group velocity (v), and the mean free path (l), i.e., $\kappa \sim Cvl$. While the assumptions of classical mechanics are inadequate to explain electron motion, due to the spin degree of freedom, classical modeling is typically considered adequate for phonons.

It then naturally follows that a reduction of any of the constituent terms would reduce the κ. As such, a reduction cannot be surmised from an elementary formulation of the Fourier heat conduction problem and various phonon transport models have then been considered[7]—ranging from the "gray" approximation where all the phonons (both acoustic and optical) are taken as equally contributing to the heat transport to "semi-gray" models[2,8] where mostly longitudinal acoustic (LA) phonons contribute while optical phonons are relatively non-contributing/stationary due to their small dispersion and group velocity. Concomitantly, there is a relative partitioning of the C values between the acoustic and optical phonons. A further improvement on the previous considerations arises through consideration of the phonon dispersion in the first Brillouin Zone (BZ), typically considered isotropic,[9] through polynomial fits to the experimental spectra.[10] The resulting frequency (ω)—wave vector (k) curve fits can then be utilized to determine the frequency dependent v while the C can be estimated through taking the temperature derivative of the total energy obtained by integrating the fits over the BZ.[6] However, the remaining factor in the thermal conductivity expression, l is not amenable to analytical calculation/fitting as it depends on the influencing[11] intimate details of the underlying material, such as anharmonic interactions, defects and impurities, surface corrugation, etc., which are rarely the same in any two individual material structures. The sensitivity of the l to such details is quite difficult to determine theoretically and, due to its importance in determining the κ, needs to be experimentally probed. For example, when one considers the l as a vector, with decomposition into three orthogonal components in a rectangular coordinate system, i.e., l_x, l_y, and l_z, there would be three corresponding values of the κ: κ_x, κ_y, and κ_z. Limits to l could be also considered, e.g., in terms of the mean free path and particular phonon wavelength, especially when the relevant component(s) approach the carrier mean free path.[10,12–14] Presently, there are very few reports on the experimental determination of the thermal conductivity tensor,[15] and typically, the isotropic value is suggested even for lower dimensional structures such as carbon nanotubes[16] where anisotropy is obviously present. It is then of interest to explore experimental methods for the determination of the κ tensor, which could yield insight into the validity of the isotropy assumption. It could be reasonably expected that the effects of anisotropy would be increasingly manifest in lower symmetry crystal structures as well as lower dimensional materials, such as thin films or nanowires.

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B. Measurement of in-plane and cross-plane thermal conductivity

We consider exploring anisotropy in thermal conduction through investigating thin films of silicon. In addition to its immense technological usage, silicon can be configured industrially in silicon-on-insulator (SOI) structures, where Si thin films can be prepared with varying thickness on an underlying oxide of low thermal conductivity (~1.4 W/mK). The advantage of the SOI manifold is that the Si thin films can be considered to be approximately thermally independent of the underlying structure. However, it should be noted that while the Si films are typically close to single-crystalline, processing could introduce random defects/impurities. In addition to enabling easier experimentation (the alternative would be to suspend the Si through complicated etching procedures), the SOI structure is commercially used in electronic devices with feature lengths <100 nm, where it has been indicated that up to a 25% increase in speed concomitant with a 50% reduction in the consumed power is achievable.[17] However, enhanced electronic switching performance is typically coupled with increased heat production,[18] the dissipation of which is a major issue with SOI based structures.

It is then of much scientific and technological interest to investigate thermal conduction issues through Si thin films in SOI structures. This involves first, the determination of both the κ_{cp} and κ_{ip} (cross- and in-plane thermal conductivity, assuming that in-plane conduction is isotropic). Typically, the experiments involve periodic surface heating—at an angular frequency—ω, through an electrical resistor, e.g., as in the 3ω method[19] where a metal line serves as both the heater and the thermometer, or through the use of a pump laser, e.g., as in time domain thermoreflectance (TDTR)[20,21] or frequency domain thermoreflectance (FDTR).[22] The thermal conductivity is deduced through an analysis of the measured signal, e.g., the third harmonic of the voltage in the 3ω method or through the change in reflectance of the surface from a probe laser in TDTR, the physical basis of which is the spread of the thermal wave in the underlying films/layers. While heat from a point source would diffuse radially, the use of metal lines of finite width or pump laser spot diameters of much greater than the thermal penetration depth (TPD) $\sim \sqrt{\frac{\kappa}{\omega\rho C}}$, results in quasi-one dimensional heat transfer and the probing of the κ_{cp}. A few corrections to the measurement of the κ_{cp}, to account for the degree of orthogonal heat flow have been described[5] to understand the relative influences of the TPD, heater width, underlying layer thickness thermal conductivity anisotropy, and other geometry dependent factors for the 3ω method. Alternatively, in TDTR/FDTR methods, the effects of heat accumulation (e.g., when the material does not reach its unperturbed state between two successive laser heating pulses) on radial heat transfer have been probed[23] and used to extract the in-plane and cross-plane thermal conductivity values of highly oriented pyrolytic graphite (HOPG). Generally, a greater sensitivity to lateral heat spreading would be achieved with an underlayer of low κ due to the slower diffusion of heat from the heating spot.

While the above state-of-the-art methodologies may yield some indication of the anisotropy of the thermal conductivity, they nevertheless provide an indirect measure. It would be desirable to develop a simpler method for measuring the anisotropy in any material, which is the broad objective of this work. Through a survey, we were convinced that correlating the changes in the optical reflectance to the temperature[24] would be most suitable, as it provides a noncontact method and mitigates issues such as boundary resistances and heater capacitances.[25] The collateral difficulties are the sensitivity of the measured signal to surface conditions and wavelength.[26] Nevertheless, we use the SOI structure as a practical platform to consider thermal conductivity anisotropy through thermoreflectance (TR) measurement.

Previous measurements of the lateral thermal conductivity of Si thin films in SOI structures mainly used electrical resistance thermometry in the steady state,[27,28] where temperature variation at two distinct points (via *in situ* fabricated highly doped areas in the Si films) was measured using an electrical resistance change. Subsequently, the κ was fit using two-dimensional heat conduction models. In another effort,[29] measurements on suspended Si thin film membranes, fabricated through wet etching techniques were performed. However, this methodology requires comparison with a metal heater deposited on a suspended bridge, with and without the Si device layer present, and thermal contact issues related to the sensors could still be significant in the characterization of κ_{ip}. A scanning thermoreflectance technique was also suggested[30] to monitor the transient temperature distribution along the drift region of a SOI power transistor. However, a discrepancy in the trend of values in the earlier data[27,28,31] with values in later measurements and theory[29] was noted.

In this paper, we expand on the utility of the TR technique to monitor the κ_{ip} of Si thin films (in the 68–258 nm range) in SOI based structures. The experimental method is aimed to avoid thermal contact related issues through the use of the thermoreflectance based temperature sensing. While the details will be exemplified later, briefly, the surface temperature gradient in the thin film induced through on-layer heating is monitored. We have then observed that the thermoreflectance, in the visible wavelength range, on SOI structures must be carefully calibrated and understood considering the optical interactions and interferences due to reflections from multiple interfaces, i.e., air-Si, Si-SiO_2 (the buried oxide layer—BOX), and the SiO_2–Si substrate, all of which are involved in the correlation of the measured TR intensity to the actual sample temperature. The optical characteristic matrix (OCM)[32] was then calculated to predict the device layer thickness at which the TR response is optimal, considering the probe wavelengths[33,34] and overlayer thicknesses.[33–37] A finite-element model based physics solver was used to estimate the temperature profile in the SOI structure with κ_{ip} of the device layer as the *only* free parameter to fit the calculated surface temperature to the measured data. Finally, the determined κ_{ip} were compared to theoretical predictions,[12,13,38,39] and the potential applications of the developed method discussed.

II. CHARACTERISTICS OF THERMOREFLECTANCE FROM SI THIN FILMS—MODELING AND CALIBRATION

The general principle of the thin film κ measurement is that when the surface is heated in a localized region, the

temperature distribution in the sample away from the heated region would be a sensitive function of the material properties, such as κ_{ip}. The temperature change (ΔT) would be measured through an optical reflectance, ΔR, change,[40] with the normalized TR response expressed through a coefficient, $C_{TR} = \frac{1}{R}\frac{dR}{dT}$. There are few published values of C_{TR}, even for bulk materials, as the sign and magnitude can vary significantly with the wavelength of incident light and sample surface quality. For example, the measured C_{TR} of Au is typically less than $10^{-4}\,\mathrm{K}^{-1}$ in the visible wavelength regime, except in the 450 nm to 575 nm range where there are peaks (up to $6\cdot10^{-4}\,\mathrm{K}^{-1}$) and zeros at ~500 nm.[33,41,42] In addition to surface roughness and contamination effects, any overlayer could also modify the spectral response of the TR, due to internal reflections and interference effects.[33–35] Consequently, it is often preferred in practice, to predict the C_{TR} using analytical methods, through knowledge of the temperature variation of the refractive index ($\tilde{n}$) and thermal coefficient of expansion. For example, in the pertinent case of a Si substrate with a SiO_2 overlayer, the C_{TR} has been derived as a function of thickness of the overlayer.[35] The reasonable agreement of the calculated values with experimentally measured results suggests that the former can be sufficient for estimation of the overlayer and spectral dependence of the C_{TR}.

The typical challenges associated with experimental TR measurements on SOI based structures are related to the (1) inadequate signal to noise ratio, given typical C_{TR} values of <0.001, (2) deconvoluting the TR contribution of the top Si film/device layer from the underlying layers and substrate, and subsequently (3) correlating the TR intensity to a relative or absolute temperature change. While the issues associated with (1) could in principle be overcome through averaging, the poor thermal conductivity of the buried oxide (BOX) is a complicating factor. We consider (2) through calculating the sensitivity of the TR intensity to the thickness and temperature of the top device layer. We then show that the TR signal intensity could be maximized through deliberate selection of a device layer thickness through evaluating the optical interactions in the SOI structure.

We chose an interrogation wavelength (λ) corresponding to visible light, i.e., $\lambda = 633$ nm, with geometry as specified in Figure 1 with appropriate parameters[43–45] for the Si ($\tilde{n} \sim 3.92 + 0.022i$, $d\tilde{n}/dT \sim 4.5 + 0.073i\,\mathrm{K}^{-1}$) and SiO_2 (Refs. 43 and 46) ($\tilde{n} \sim 1.457$ and $d\tilde{n}/dT \sim 10^{-5}\,\mathrm{K}^{-1}$). The top/device layer is single crystalline Si (with thicknesses, t_{dev}, in the range of 68–258 nm, and resistivity ~1–10 Ω cm), with an underlying 1 μm SiO_2 (BOX) layer, supported by a ~675 μm thick single crystal Si substrate. From an optical standpoint, the electromagnetic skin depth,[32] d_{Si}, of Si, at $\lambda = 633$ nm, is ~2.3 μm, which indicates that incident radiation would penetrate through the Si device layer. The BOX layer is transparent and was modeled with only a real component to $\tilde{n}$, while the substrate is much thicker than d_{Si} and is optically opaque.

If the incident radiation, modeled as a electromagnetic plane wave and represented through $Q_0 = \begin{bmatrix} E_0 \\ H_0 \end{bmatrix}$, with E_o and H_o as the free-space amplitudes of the electric and magnetic fields, is incident upon a slab of material with refractive

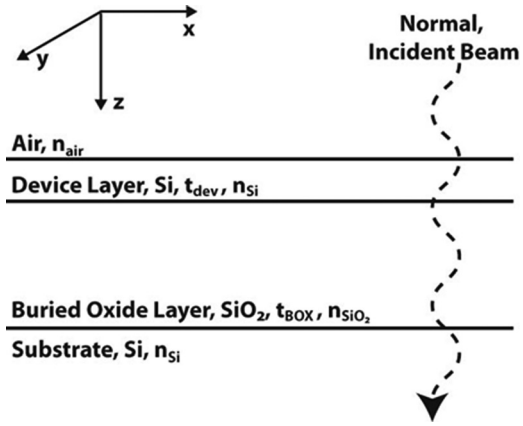

FIG. 1. Schematic of the SOI samples studied in this work. The optical parameters governing the beam-material interactions, *n*: refractive index and *t:* the material thickness, are indicated.

index $\tilde{n}_s$, the resultant amplitude at depth z within the slab is given by $Q = \begin{bmatrix} E(z) \\ H(z) \end{bmatrix}$, where $Q = M_s Q = Q_0$. The electric and magnetic fields are taken to be of the forms: $E_x = E(z)e^{i(kz-\omega t)}$ and $H_y = H(z)e^{i(kz-\omega t)}$, respectively. M_s is the optical characteristic matrix (OCM) of the layered slab, comparing the amplitude of the propagated wave to that of the initial state, and for normal incidence, is

$$M_s(z) = \begin{bmatrix} m_s^{11}(z) & m_s^{12}(z) \\ m_s^{21}(z) & m_s^{22}(z) \end{bmatrix} = \begin{bmatrix} \cos\left(\frac{2\pi\tilde{n}_s z}{\lambda}\right) & -\frac{i}{\tilde{n}_s}\sin\left(\frac{2\pi\tilde{n}_s z}{\lambda}\right) \\ -i\tilde{n}_s \sin\left(\frac{2\pi\tilde{n}_s z}{\lambda}\right) & \cos\left(\frac{2\pi\tilde{n}_s z}{\lambda}\right) \end{bmatrix}. \quad (1)$$

For SOI structures, the M_{SOI}, is equal to the product of the individual OCMs of each optically active layer, i.e., the top Si device layer (*dev*) and the SiO_2 (*BOX*).

$$M_{SOI}(z) = M_{dev}(z)M_{BOX}(z). \quad (2)$$

It can then be shown[32] that the total reflectance of the SOI structure, R_{SOI}, is

$$R_{SOI} = \left|\frac{(m_{SOI}^{11} + m_{SOI}^{12}\tilde{n}_{sub})\tilde{n}_{air} - (m_{SOI}^{21} + m_{SOI}^{22}\tilde{n}_{sub})}{(m_{SOI}^{11} + m_{SOI}^{12}\tilde{n}_{sub})\tilde{n}_{air} + (m_{SOI}^{21} + m_{SOI}^{22}\tilde{n}_{sub})}\right|^2. \quad (3)$$

A plot of R_{SOI} as a function of the device layer thickness (t_{dev}) at $\lambda = 633$ nm is shown in Figure 2 along with obtained experimental results, and the close correspondence for the chosen thicknesses (the reason for the choice is explained later in this section) indicates the accuracy of our modeling and experimental calibration. The peaks and troughs in the R_{SOI} are due to interference effects of the incident radiation from the device layer boundaries. The shape of the variation, i.e., broad peaks and narrow troughs, are due to a large refractive index contrast ($\tilde{n}_{dev} - \tilde{n}_{BOX} \sim 2.5$) between the Si device layer and the underlying oxide, and the periodicity is determined by one quarter of the optical path length ($t_{dev}\tilde{n}_{dev}$), due to constructive and destructive interferences.

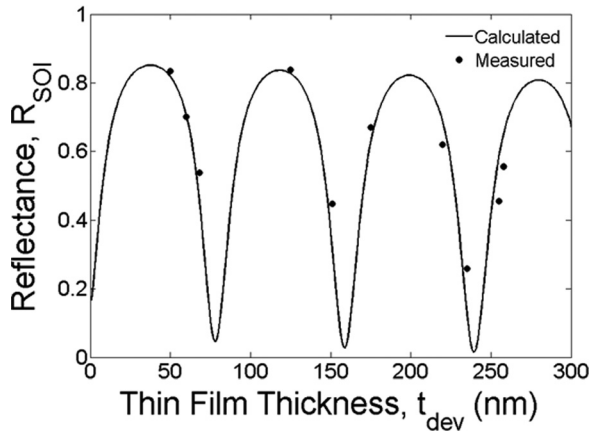

FIG. 2. The calculated and measured optical reflectance (R_{SOI}) of the SOI samples, with varying device layer thickness (t_{dev}).

It was then inferred from the R_{SOI}–t_{dev} variation, that the C_{TR} (or $\frac{dR}{dT}$) could be increased at an optimal t_{dev}. Generally, when any layer of thickness t has a temperature variation ΔT, the change of the refractive index and thickness would be $\Delta\tilde{n} = \frac{d\tilde{n}}{dT}\Delta T$ and $\Delta t = \xi \Delta T$, respectively, where ξ is the linear thermal coefficient of expansion. For a given SOI sample with a specified device layer thickness, t_{dev}, and an initial temperature, T^0, with reflectance R (T^0, t_{dev}), the net change in the reflectance, ΔR, is written as

$$\Delta R = \frac{dR}{dT}\Delta T = R\left(T^0 + \Delta T, t_{dev} + \Delta t,\right) - R\left(T^0, t_{dev}\right). \quad (4)$$

For a unit rise in ΔT (=1 K), and using Eq. (4), a plot of ΔR vs. the t_{dev} was formulated (as in Figure 3), to show the individual $\frac{dR_i}{dT}$ (i = dev, BOX, or substrate) due to uniform temperature rise for the ith layer. From an experimental point of view, we model the observed $\frac{dR}{dT}$ of the SOI structure as arising due to a linear superposition of the individual layers, as follows:

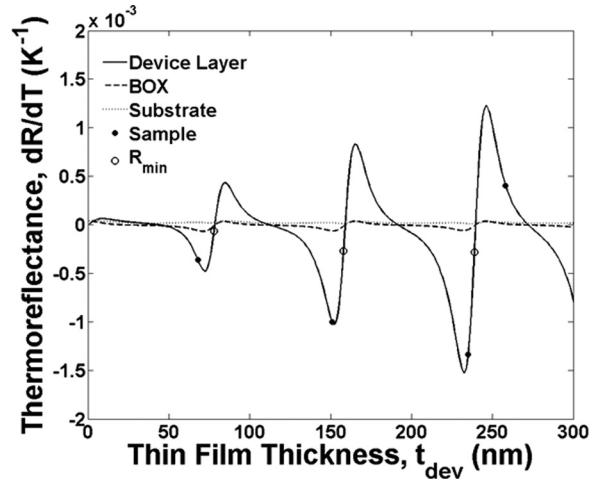

FIG. 3. The variation of the temperature derivative of the reflectance (dR/dT) with device layer thickness (t_{dev}) for the individual layers of the sample, including the top device layer, underlying buried oxide (BOX) and the substrate. The values corresponding to the t_{dev} of the measured samples (Sample) and the minima (R_{min})—from Figure 2, are indicated.

$$\frac{dR_{SOI}}{dT} = \frac{dR_{dev}}{dT} + \frac{dR_{BOX}}{dT} + \frac{dR_{sub}}{dT}. \quad (5)$$

Such a model is necessary as the individual contributions of the layers of the SOI are not measurable and was justified on the basis of our observation, through computational simulations using MATLAB®, that the difference of $\frac{dR_{SOI}}{dT}$ between (i) that found by considering and summing the individual contributions from each layer (each with a $\Delta T = 1$ K) and (ii) assuming that that SOI structure as a whole has $\Delta T = 1$ K, is less than 1%.

The following were then observed from the plot: (1) there was a pronounced modulation of the $\frac{dR_i}{dT}$, which could be either positive/negative, and which is of the same sign as the slope of R_{SOI}; (2) the $\frac{dR_{dev}}{dT}$ dominates that of the other layers by two orders of magnitude ($10^{-3}\,K^{-1}$ vs. $10^{-5}\,K^{-1}$) resulting from both the position of the device layer and the much larger $\frac{d\tilde{n}}{dT}$, and would be the chief contributor to the TR intensity; (3) The modulation of the $\frac{dR_{dev}}{dT}$ increases in amplitude with t_{dev} and exhibits a maxima whenever there is a minimum in the R (cf. Figure 2), with the experimental implication that there are select values of t_{dev} where the $\frac{dR_{dev}}{dT}$ is maximum/minimum with corresponding effect on the TR intensity. Consequently, the Si thin film thickness (t_{dev}) must be chosen carefully for maximal signal to noise ratio in the TR measurements, to enable more accurate determination of the κ. We have then chosen Si thin films with $t_{dev} = 68$ nm, 151 nm, 235 nm, and 258 nm corresponding to thicknesses near the maxima of the absolute $\frac{dR_{dev}}{dT}$ as indicated in Figures 2 and 3.

III. EXPERIMENTAL PROCEDURES

Si thin films of optimal t_{dev} following the discussion of the previous section, were fabricated on SOI based wafers (from SOITEC, made using a bond and etch-back (BESOI) technique) through reactive ion etching (RIE, using the Oxford Plasmalab® 100) of the as-received structures. On the as-received SOI structures, the Si crystalline device layer (258 nm thick) was (100) oriented, p-type (1–10 Ω cm), with an underlying BOX layer of 1 μm thickness. The electrical dopant density of $\sim 10^{15}$ atoms/cm[3,47] was not expected to much affect the κ.[48] Measurement and calibration of film thickness was done through spectral reflectance (Filmetrics F20) and error in the measurement was estimated to be less than 5 nm. The surface roughness introduced during the RIE was of the order of a few nanometers. A metal line was then deposited on the Si film surface to serve for an electrical resistance based heater. For this purpose, the heater pattern was transferred through a double-layer photolithographic technique, employing the following procedures: (1) 400 nm of photoresist (Nano PMGI SF8) was spun onto the sample and baked for 5 min at 180 °C, (2) 2 μm of another photoresist (Shipley 1818) was then spun on top and baked for 3 min at 110 °C. The photoresist was then exposed through a suitably designed mask (using a Karl Suss MA6 mask alignment platform) for 10 s at ~300 W. The heater line was constituted of a multilayer of Cr (10 nm)/Au (200 nm) deposited through electron beam evaporation (Temescal BJD 1800) and was

typically 10 mm long and 6 μm wide. Using double layer processing seems to ensure better contact between the heater and the device layer along the entire width.

To characterize possible current leakage from the heater into the substrate, 30 nm of SiO_2 was deposited underneath the heater line. However, measurements did not indicate any leakage effects precluding the need for such an oxide. Subsequent to the fabrication of the optimal t_{dev} films, the samples were mounted and wire-bonded to ceramic chip-carriers. Thermal epoxy was used to bond the substrate bottom to the sample holder. The overall sample configuration is schematically shown in Figure 4(a), and the setup for the measurement of the TR intensity in Figure 4(b). It was assumed that the micro-positioner, to which the sample holder was mounted, was an adequate thermal sink and fixed the sample holder bottom to ambient temperature.

A sinusoidal current *I(f)*, at a given frequency *f*, was passed through the deposited metal line and induces Joule heating (with a harmonic component of 2*f*, as derived from the I^2 component of the heating). AC modulation techniques enable accurate lock-in based detection of the effects of the induced heating with high signal to noise ratio. Thermal losses, due to convection or radiation heat transfer, were ignored through the use of time constants (and *f* values) not overlapping with the characteristic time scales associated with such loss mechanisms. Using lumped thermal analysis,[49] we estimated that for the device layer thicknesses considered in our experiments that the time scales were of the order of magnitude of 0.01–0.1 s. Consequently, we use a heating current frequency, f_h, of ~2.5 kHz and we consider only the conductive heat transfer. Also, the estimated change in the surface temperature due to convective/radiative heat loss was estimated to be less than 1%, through elementary calculations using Newton's law of cooling and the Stefan–Boltzmann Law.

At the chosen *f*, the thermal wave propagates into the Si substrate, through the top device layer and the BOX.[50] Due to the orders of magnitude lower κ and much larger thickness of the oxide compared to that of the device layer, it was assumed that there is a much larger temperature drop across the oxide. Hence, the top device layer was essentially isothermal through the thickness at any given distance from the heater. However, there seems to be significant lateral heat conduction in the BOX *near* the heater, which modifies the temperature profile of the device layer, and precludes the use of analytic expressions for the temperature distribution, as was done in earlier studies.[28] Consequently, finite element modeling was used to understand such variations, as will be discussed later (see Sec. IV B).

A normally incident, linearly polarized He-Ne laser (633 nm, 10 mW, from Thorlabs, Inc.) was then focused onto a heated sample through a 36 ×, objective lens (Ealing Inc., with a numerical aperture = 0.5). The spot size was determined through a *knife-edge* technique, where the beam was scanned over the metal heater edge onto the Si film surface. Assuming a Gaussian beam profile, with intensity variation given through $I(x) = I_0 \exp\left(\frac{-x^2}{2r^2}\right)$, the spot radius, *r*, was found to be ~4 μm. The effect of deviations from normal incidence on the OCM (from Eq. (4)) was characterized, and it was seen that there was a small upwards shift of the TR (see Figure 3). For recording the spatial variation of the TR, the sample was translated, with 0.2 μm resolution, rastering the focused laser spot across the surface. The reflected intensity was diverted—see Figure 4(b)—through a non-polarized beam splitter onto a diode detector (ThorLabs DET110A) connected to a lock-in amplifier (Stanford Research Systems SR 830) synchronized to 2*f*. Both the amplitude (proportional to the temperature fluctuations of the surface) and the phase (related to the sign of the C_{TR}) of the signal were recorded as a function of distance from the heater. The obtained values in the TR measurement were limited by the dark current noise of the detector, of the order of 4 nA.

IV. RESULTS AND DISCUSSION

A. Determination of the specific heat, *C*, and the phonon group velocity, v_g, for device layer

A suitable value for the density (ρ) and the specific heat (*C*) constituting the thermal diffusivity, $D(=\frac{\kappa}{\rho C})$ of the device layer was necessary prior to solving/modeling the transient heat conduction equation. While the density was assumed to be that of the bulk,[43] $\rho_{Si} = 2329\ \mathrm{kg/m^3}$, the bulk value of $C \sim 1.67 \cdot 10^6\ \mathrm{J/m^3\,K}$ associated with the "gray" approximation of phonons,[51] in which all phonons are treated identically, does not consider their dispersion. A more appropriate value of *C*, which does account for the

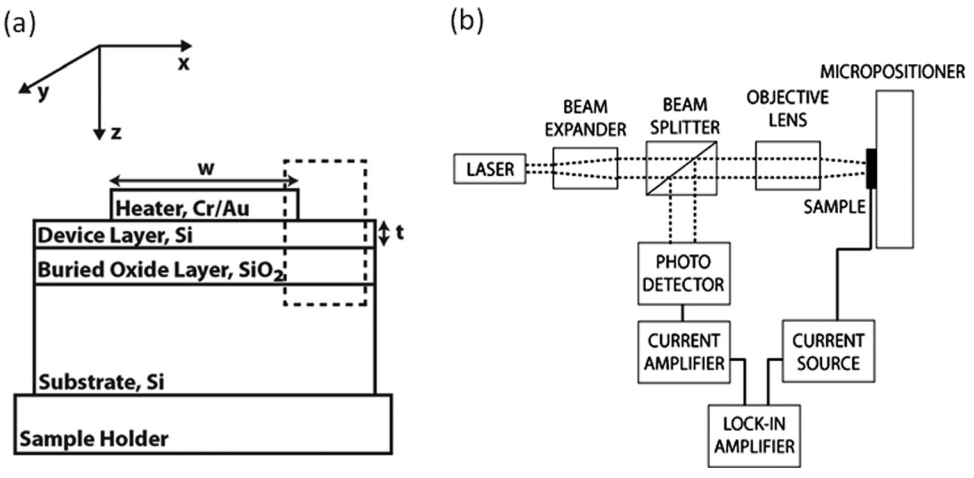

FIG. 4. (a) Schematic of the cross-section of the measured samples with the heater, which was mounted on a chip carrier. The lateral heat flow, in the *x*-direction, in the region delineated by the dotted box, is sensitive to the in-plane thermal conductivity (κ_{ip}) and the corresponding temperature variation along the surface has been measured. (b) Schematic of the arrangement of apparatus used for the scanning thermoreflectance thermometry.

phonon dispersion, was derived through previously developed methods.[12,13,38,39] To illustrate, it was assumed that only the acoustic phonons contribute to heat conduction, while the optical phonons do not, due to their small group velocity, and that the C associated with heat conduction would be that appropriate for the former group. The full phonon dispersion in Si consisting of one longitudinal and two degenerate transverse modes (i.e., LA, TA and LO, TO modes) was considered. Using polynomial fitting functions to analytically describe the experimentally measured acoustic phonon dispersion,[52] we calculated a $\bar{C}_{avg} \sim 0.95 \cdot 10^6\,\mathrm{J/m^3\,K}$ under the Debye model formulation.[6] We also estimated an average phonon group velocity, $\bar{v}_g$, by including the dispersion and normalizing, as follows:

$$\bar{v}_g = \frac{C_{LA} v_{g,LA} + 2C_{TA} v_{g,TA}}{\bar{C}_{avg}}. \tag{6}$$

The resulting analysis yields $\bar{v}_g = 2274\,\mathrm{m/s}$, which is notably smaller than the value typically considered for bulk, i.e., $\sim$6000 m/s. Taking a κ value for Si ($\sim$140 W/mK), $\bar{v}_g$, and $\bar{C}_{avg}$, we obtain an average value of the mean free path, $\bar{l}_{avg} \sim 200\,\mathrm{nm}$, implying more phonon-boundary interaction in thin films than traditional thermal analysis suggests. Thus, a reduction of κ_{ip} at film thickness near or less than $\bar{l}_{avg}$ would be expected. Such a framework to understand the reduction of the in-plane thermal conductivity, κ_{ip}, in Si thin films[14,29,53] and the device layer in SOI substrates[28,54] has been previously established and agreed well with our calculations. Our experimental results[55] also indicated that considering the full phonon dispersion was more accurate.

B. Finite element modeling

As noted earlier, the SOI geometry along with the large aspect ratio of the heater width ($\sim$24) vis-à-vis the device layer thickness (typically, $t_{dev} < 250\,\mathrm{nm}$) implies a decaying temperature profile from the heater edge in the x-direction, following Figure 4(a). Consequently, a two-dimensional analysis of the heat conduction along the cross-section of the sample, perpendicular to the heater axis (i.e., the x–z plane), was pertinent. The Fourier heat conduction equation was solved through a finite element model (FEM) constructed in the COMSOL Multiphysics® software environment, to determine the time varying temperature along the surface of the device layer in the proximity of the heater and, for analyzing the sensitivity of the device layer κ_{ip}. By choosing appropriate free parameters, the calculated temperature profiles could be *fit* to the measured TR data to elucidate the thermal properties of the device layer.

In accordance with experimental conditions, the following assumptions were used in the model: (1) the heat sink fixes the bottom substrate surface to room temperature, $T_{bottom} \sim 293\,\mathrm{K}$; (2) sample surfaces exposed to air were taken to be insulating, i.e., $\left(\frac{dT}{dx}\right)_{surface} = \left(\frac{dT}{dz}\right)_{surface} = 0$; (3) the power per unit area dissipated by the heater at the heater/device layer interface was equal to Joule heat generated by the heating current; and (4) the BOX and Si substrate have bulk thermal properties. The sensitivity of the model solution was examined with respect to the cross-plane thermal conductance, heating power, and frequency. It was found that the surface temperature was unperturbed by variation of the device layer κ_{cp} considered in this work, as well as from the introduction of thermal boundary resistances at the device layer/BOX and BOX/substrate interfaces, using commonly accepted values.[1] The thermal epoxy between the substrate bottom and the sample holder could introduce a resistance in series with the sink and was estimated to be $\sim 10^{-3}\,\mathrm{m^2\,K/W}$. However, introduction of the boundary resistance in the model had negligible effect on the transient component of the surface temperature, as the chosen f limits the thermal penetration depth to $\sim$75 μm in Si, precluding the interaction of the thermal wave with the bottom of the substrate. Additionally, variation of the heating power and frequency within the limits of specified machine error, $\sim$0.1%, did not yield a change in the surface temperature greater than the obtained precision. An example of the calculated temperature profile along the sample cross section near the peak of the heating cycle is shown in Figure 5(a).

C. Experimental measurements of the lateral temperature variation on device layer surface

A typical TR scan, across the surface of the device layer ($t_{dev} = 258\,\mathrm{nm}$), indicating the experimental data superposed on calculated temperature profiles with varying κ_{ip}, is shown in Figure 5(b). Each datum represents the maximum amplitude variation of the TR intensity as it varies in time at frequency $2f$, and whose x-coordinate coincides with the center of the probe beam. The error bars due to variation of the TR intensity are also labeled, but are *too small* to be visible. The magnitude of the TR intensity was scaled such that the values in the limit of $x \to \infty$, e.g., when $x \sim 40\,\mu$m in Figure 5(b), match the calculated temperature. While the total TR intensity was an average of the temperature profile convoluted with the spatially distributed intensity of the beam, the resulting measurement was still an accurate indication of the actual temperature at the center of the beam spot.[55] The solid curves represent equivalent, time-variant temperature amplitudes as a function of distance from the heater edge at various modeled κ_{ip}. The goodness of fit between the measured results and simulated curves was determined in the range of spatial values where modeled temperature profiles diverged by more than 10%, i.e., at $4\,\mu\mathrm{m} < x < 30\,\mu\mathrm{m}$. The largest correlation coefficient between the scaled TR measurements and calculated temperature values was $R^2 = 0.9999$, corresponding to the fit with $\kappa_{ip} \sim 100\,\mathrm{W/mK}$. It was noted that the values of κ_{ip}, matching 60 and 148 W/mK, have R^2 values of 0.9955 and 0.9978, respectively. While correlation remains high for the given calculated temperature profiles, their relative values could be used to indicate the most appropriate κ_{ip} so as to closely match experimental data.

Figure 5(c) shows the measured TR signal phase of the heat wave peak as a function of the distance from the heater, where decreasing phase indicates greater lag with respect to the heating frequency reference. The phase was a direct indication of the difference in sign of $\frac{dR_{dev}}{dT}$ between samples of different thickness (cf. Figure 3). More specifically,

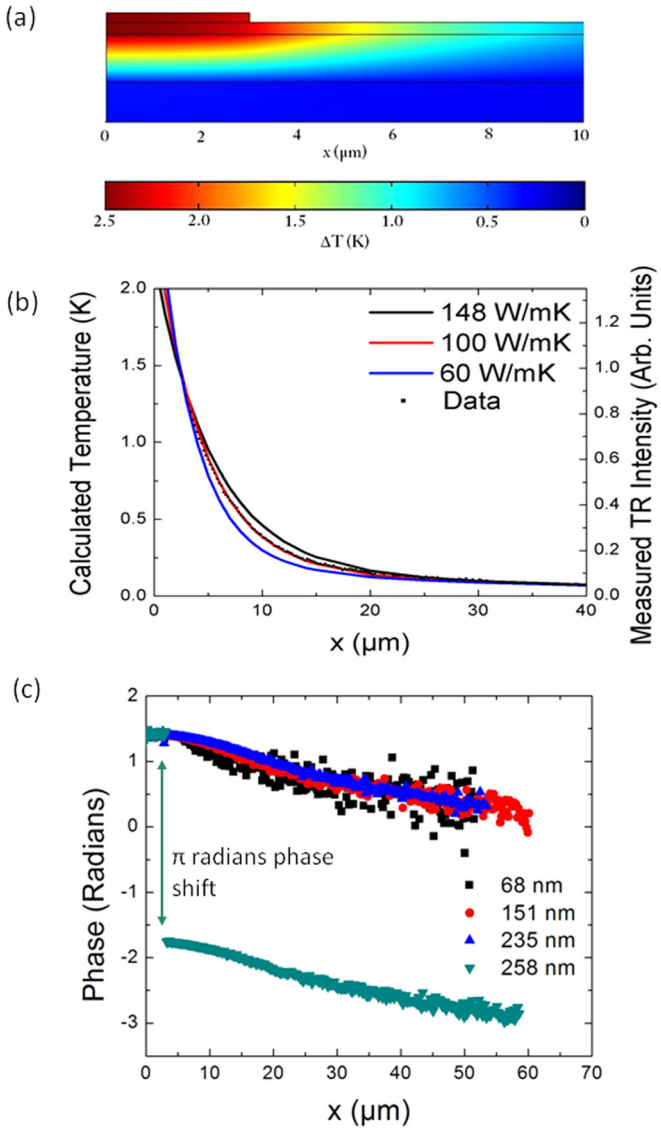

FIG. 5. (Color online) (a) Modeled variation, through FEM, of the temperature along the sample cross-section, indicated at the peak of a given heating cycle. (b) A typical TR scan across the surface of the device layer ($t_{dev} = 258$ nm) indicating the experimental data superposed on modeled temperature profiles with varying κ_{ip}. The error bars are *too small* to be visible. (c) The measured TR signal phase of the heat wave peak as a function of the distance from the heater is a direct indication of the difference in sign of TR intensity between samples of different thickness (cf. Figure 3)

comparing the signs of the $\frac{dR_{dev}}{dT}$ for $t_{dev} = 258$ nm to other device thicknesses, i.e., $t_{dev} = 68$, 151, and 235 nm, the former has a positive value while the latter have negative values. Consequently, the lock-in measurement of two TR signals with identical phase but opposite sign would be manifested in a π radians phase shift, as indicated in Figure 5(c). It was also noted that the TR signal phase did not indicate a π phase shift as the beam was rastered from the Au heater line to the device layer, implying that $\frac{dR_{dev}}{dT}$ and $\frac{dR_{Au}}{dT}$ were of the same sign for samples with $t_{dev} = 68$, 151 and 235 nm. As it was previously established that $\frac{dR_{Au}}{dT}$ is negative at $\lambda = 633$ nm,[33,41,42] the $\frac{dR_{dev}}{dT}$ of these SOI samples at these thickness must be negative as well, further supporting the OCM predictions plotted in Figure 3.

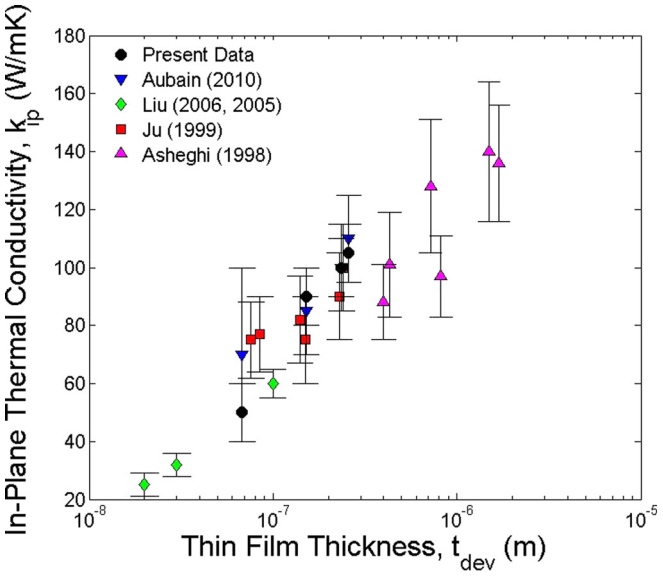

FIG. 6. (Color online) A comparison of the thermal conductivity values (obtained from the TR intensity fits in the present work) with those obtained previous literature (Aubain *et al.*,[55] Liu *et al.*,[29,57] Ju *et al.*,[31] Asheghi *et al.*[28]).

D. Estimation of the κ_{ip} of Si thin films

The principles outlined above were used to determine the values of the thermal conductivity and compare with those obtained by other previous measurements[31,55] and plotted in Figure 6. Generally, a decreasing κ_{ip} is observed with decreasing to t_{dev}. The high accuracy and precision of the data obtained in this work—as in Figure 5(b), stems from the accuracy in modeling as well as improved spatial resolution. Most notably, there seems to very good agreement between our measured κ_{ip} and those obtained through measurements with suspended Si structures fabricated from SOI substrates.[56] Generally, suspended beam geometry greatly simplifies thermal analysis due to the restriction on heat conduction paths. However, fabrication of such geometries is elaborate and non-trivial involving highly controlled wet etching and is often not easily implemented for many thin films of interest, e.g., those lacking a sacrificial intermediate layer. The comparison of the κ_{ip} previously measured through electrically resistive elements of suspended[56] and supported[27,28,31] Si films show that measurements of supported samples seem to be less sensitive to the film properties[31] or have high variability.[28]

V. SUMMARY

The in-plane thermal conductivities of Si thin films, ranging, from 68 nm to 258 nm in thickness on SOI substrates, were recorded using a TR based optical technique measuring heat conduction along the surface. The TR response (both the magnitude and the sign) was found to be sensitive to the thickness of the top Si device layer and modeled using an optical characteristic matrix formulation to choose appropriate thin film thicknesses. High aspect ratio, on-chip heating elements produced temperature profiles that were measured as a function of distance with respect to the heater edge, and the profiles were fit to a robust finite

element model with κ_{ip} as the only free parameter. Comparison of the obtained thermal conductivity values with previous measurements confirms the validity of the technique and suggests that complete isolation of the Si thin film from the substrate may not be required for extracting κ_{ip}.

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